



PIMZ2-Q

NPN/PNP general-purpose double transistor

26 February 2025

Product data sheet

1. General description

NPN/PNP general-purpose double transistors in a very small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Simplified circuit design
- Reduced component count
- Reduced pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- General-purpose switching and amplification

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_C	collector current		-	-	150	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	C2	collector TR2	<p>TSOP6 (SOT457)</p>	<p>sym082</p>
2	E2	emitter TR2		
3	C1	collector TR1		
4	E1	emitter TR1		
5	B1	base TR1		
6	B2	base TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PIMZ2-Q	TSOP6	plastic, surface-mounted package (SC-74; TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PIMZ2-Q	M6

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CBO}	collector-base voltage	open emitter		-	60	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	7	V
I_C	collector current			-	150	mA
I_{CM}	peak collector current			-	200	mA
I_{BM}	peak base current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^{\circ}\text{C}$	[1]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^{\circ}\text{C}$	[1]	-	300	mW
T_j	junction temperature			-	150	$^{\circ}\text{C}$
T_{amb}	ambient temperature			-65	150	$^{\circ}\text{C}$
T_{stg}	storage temperature			-65	150	$^{\circ}\text{C}$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB).

9. Thermal characteristics

Table 6. Thermal characteristics

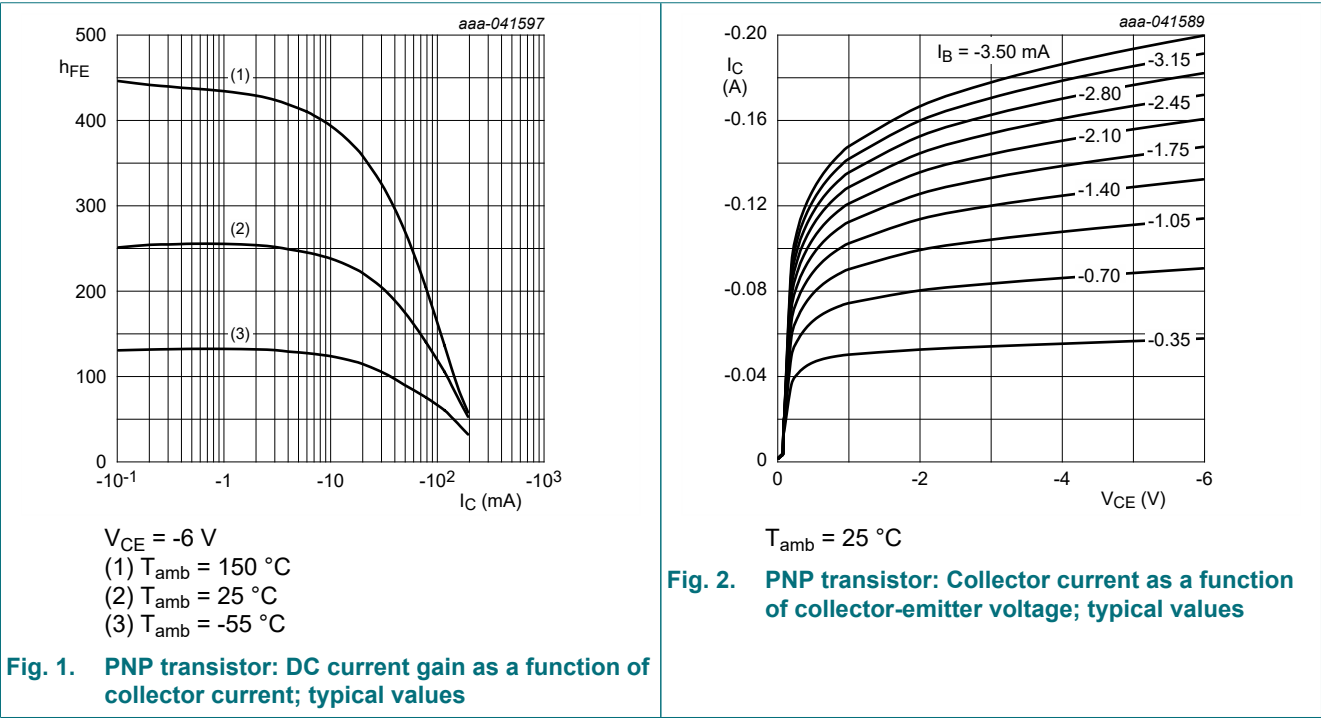
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	$T_{amb} \leq 25\text{ }^{\circ}\text{C}$	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	$T_{amb} \leq 25\text{ }^{\circ}\text{C}$	[1]	-	-	417	K/W

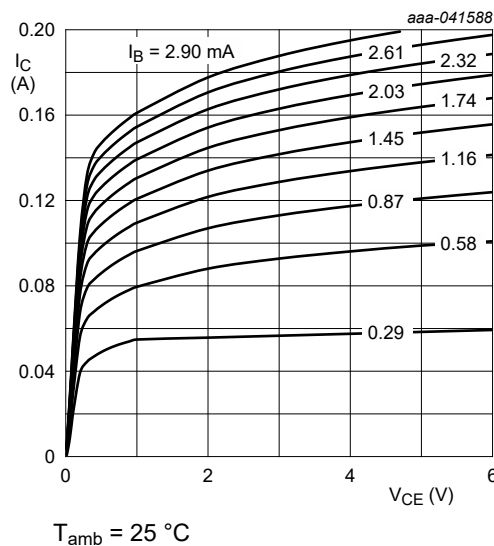
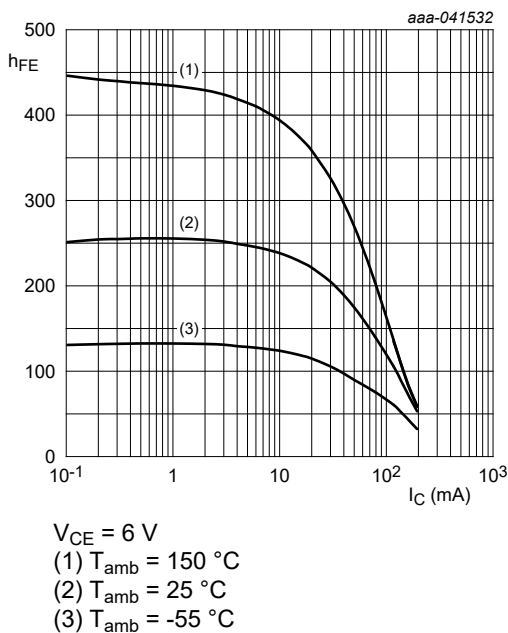
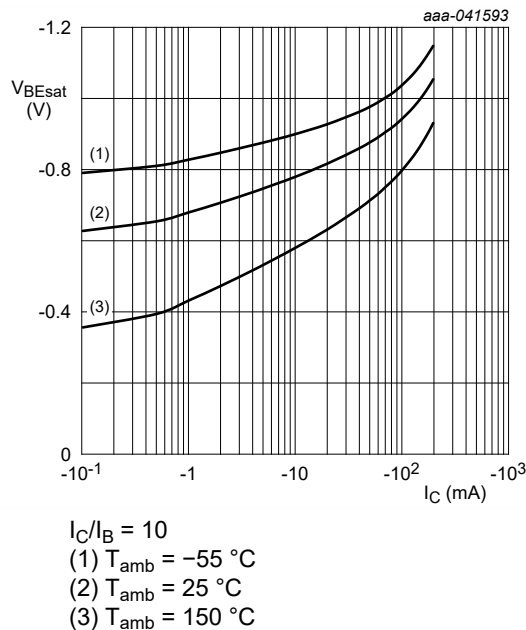
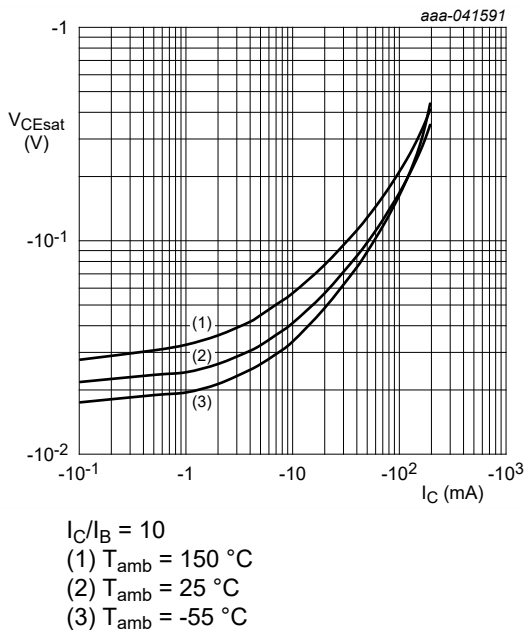
[1] Device mounted on an FR4 printed-circuit board.

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity; unless otherwise specified						
I_{CBO}	collector-base cut-off current	$V_{CB} = 60\text{ V}; I_E = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	100	nA
		$V_{CB} = 60\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ °C}; T_{amb} = 25\text{ °C}$	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 7\text{ V}; I_C = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	100	nA
h_{FE}	DC current gain	$V_{CE} = 6\text{ V}; I_C = 1\text{ mA}; T_{amb} = 25\text{ °C}$	120	250	560	
TR1 (PNP)						
V_{CEsat}	collector-emitter saturation voltage	$I_C = -50\text{ mA}; I_B = -5\text{ mA}; T_{amb} = 25\text{ °C}$	-	-	-500	mV
C_c	collector capacitance	$V_{CB} = -12\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A}; f = 1\text{ MHz}; T_{amb} = 25\text{ °C}$	-	2.3	5	pF
f_T	transition frequency	$V_{CE} = -12\text{ V}; f = 100\text{ MHz}; T_{amb} = 25\text{ °C}; I_E = -2\text{ mA}$	-	190	-	MHz
TR2 (NPN)						
V_{CEsat}	collector-emitter saturation voltage	$I_C = 50\text{ mA}; I_B = 5\text{ mA}; T_{amb} = 25\text{ °C}$	-	-	250	mV
C_c	collector capacitance	$V_{CB} = 12\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A}; f = 1\text{ MHz}; T_{amb} = 25\text{ °C}$	-	-	3	pF
f_T	transition frequency	$V_{CE} = 12\text{ V}; f = 100\text{ MHz}; T_{amb} = 25\text{ °C}; I_E = 2\text{ mA}$	100	-	-	MHz





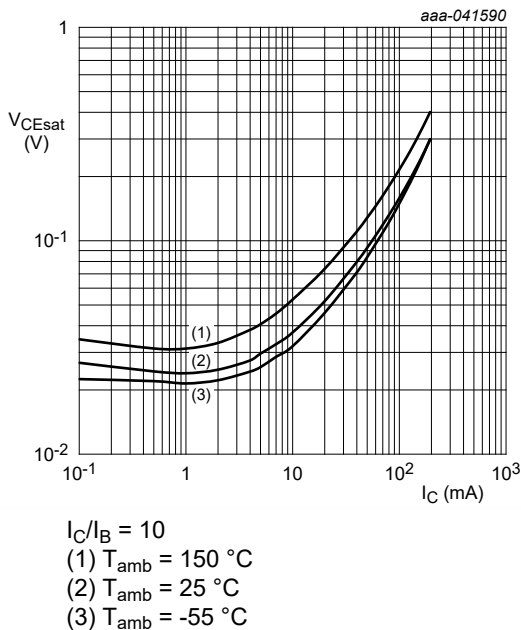


Fig. 7. NPN transistor: Collector-emitter saturation voltage as a function of collector current; typical values

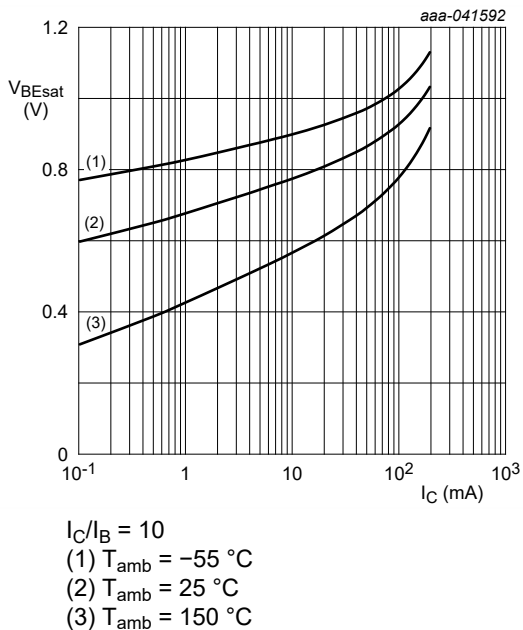


Fig. 8. NPN transistor: Base-emitter saturation voltage as a function of collector current; typical values

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

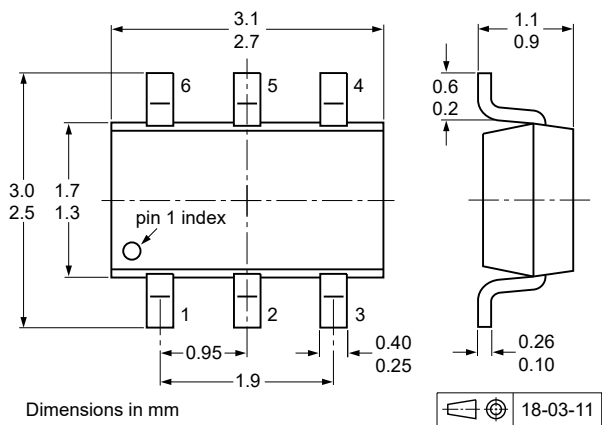


Fig. 9. Package outline TSOP6 (SOT457)

13. Soldering

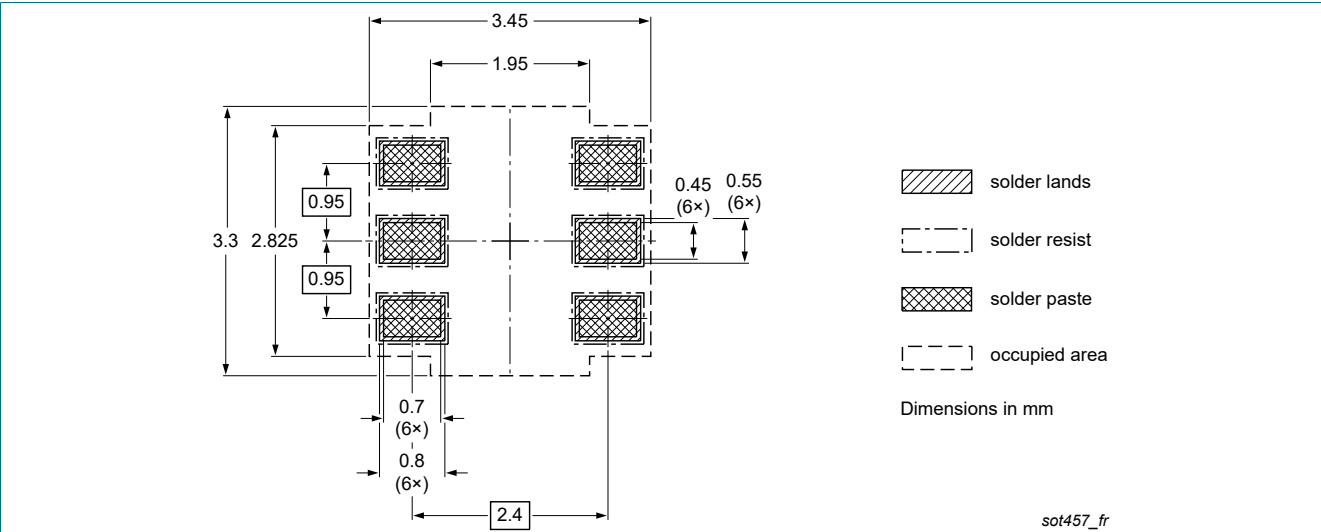


Fig. 10. Reflow soldering footprint for TSOP6 (SOT457)

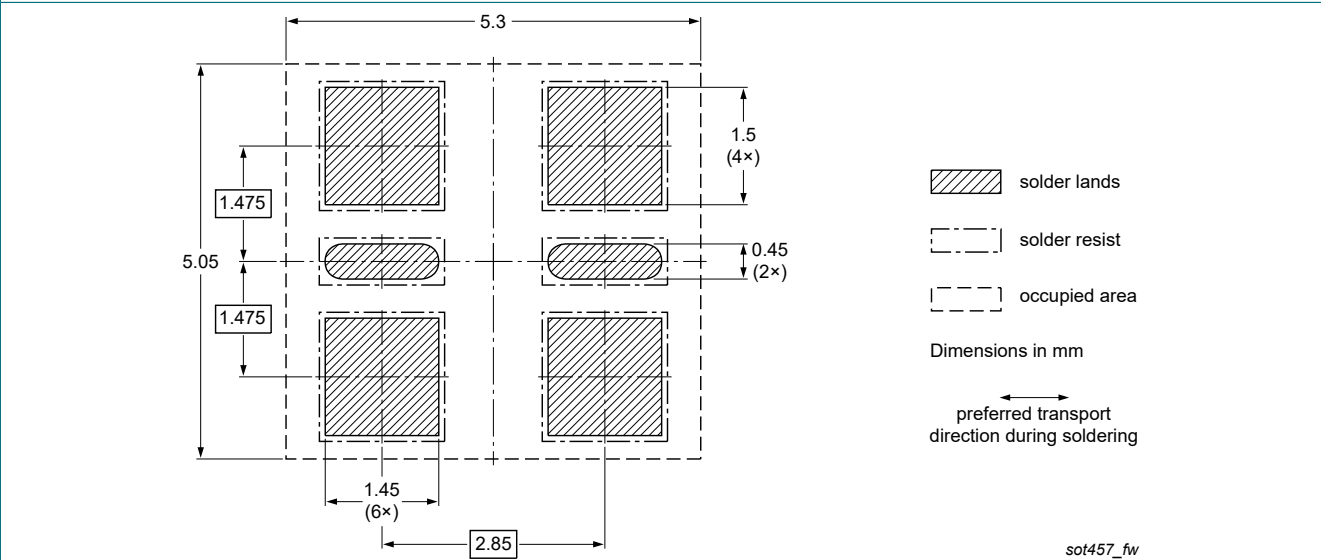


Fig. 11. Wave soldering footprint for TSOP6 (SOT457)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PIMZ2-Q v.1	20250226	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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